Abstract

A computer body outputting only address signals A0 to A11 could use only a half area of a 256-megabit SDRAM.

The memory circuit 30 receives a predetermined number of address signals A0 to A11 and a plurality of select signals CS0 and CS1, generates a memory select signal CS and an additional address signal A12 added to the signals A0 to A11 according to the inputted signals CS0 and CS1, and provides the signal CS, signal A12, and signals A0 to A11 to a 256-megabit SDRAM (memory), so that the computer body can access the corresponding data. The computer body can access the data corresponding to the generated additional address signal A12 and predetermined number of the address signals A0 to A11.